# Booth Multiplication Algorithm <br> Abenet Getahun <br> Fall 2003 CSCI 401 

## Booth Multiplication Algorithm

Booth algorithm gives a procedure for multiplying binary integers in signed -2 's complement representation.

I will illustrate the booth algorithm with the following example:
Example, $2_{\text {ten }} \times(-4)_{\text {ten }}$

$$
0010_{\mathrm{two}} * 1100_{\mathrm{two}}
$$

## Step 1: Making the Booth table

I. From the two numbers, pick the number with the smallest difference between a series of consecutive numbers, and make it a multiplier.
i.e., 0010 -- From 0 to 0 no change, 0 to 1 one change, 1 to 0 another change ,so there are two changes on this one
1100 -- From 1 to 1 no change, 1 to 0 one change, 0 to 0 no change, so there is only one change on this one.
Therefore, multiplication of $2 \times(-4)$, where $2_{\text {ten }}\left(0010_{\mathrm{two}}\right)$ is the multiplicand and $(-4)_{\text {ten }}\left(1100_{\mathrm{two}}\right)$ is the multiplier.
II. Let $\mathrm{X}=1100$ (multiplier)

Let $\mathrm{Y}=0010$ (multiplicand)
Take the 2's complement of $Y$ and call it $-Y$
$-\mathrm{Y}=1110$
III. Load the $X$ value in the table.
IV. Load 0 for $\mathrm{X}-1$ value it should be the previous first least significant bit of X
V. Load 0 in $U$ and $V$ rows which will have the product of $X$ and $Y$ at the end of operation.
VI. Make four rows for each cycle; this is because we are multiplying four bits numbers.


Load the value
$1^{\text {st }}$ cycle
$2^{\text {nd }}$ cycle
$3^{\text {rd }}$ Cycle
$4^{\text {th }}$ Cycle

## Step 2: Booth Algorithm

Booth algorithm requires examination of the multiplier bits, and shifting of the partial product. Prior to the shifting, the multiplicand may be added to partial product, subtracted from the partial product, or left unchanged according to the following rules:

Look at the first least significant bits of the multiplier " X ", and the previous least significant bits of the multiplier "X -1 ".

I $00 \quad$ Shift only
11 Shift only.
$01 \quad$ Add Y to U, and shift
10 Subtract Y from U, and shift or add (-Y) to U and shift
II Take U \& V together and shift arithmetic right shift which preserves the sign bit of 2's complement number. Thus a positive number remains positive, and a negative number remains negative.
III Shift X circular right shift because this will prevent us from using two registers for the X value.


Repeat the same steps until the four cycles are completed.

|  |  |  |  |  |
| :--- | :--- | :--- | :--- | :---: |
| U | V | X | $\mathrm{X}-1$ |  |
| 0000 | 0000 | 1100 | 0 |  |
| 0000 | 0000 | 0110 | $\mathbf{0}$ |  |
| $\mathbf{0 0 0 0}$ | $\mathbf{0 0 0 0}$ | $\mathbf{0 0 1 1}$ | $\mathbf{0}$ |  |
|  |  |  |  |  |
|  |  |  |  |  |


| U | V | X | X-1 |  |
| :---: | :---: | :---: | :---: | :---: |
| 0000 | 0000 | 1100 | 0 |  |
| 0000 | 0000 | 0110 | 0 |  |
| 0000 | 0000 | 0011 | 0 |  |
| $\begin{aligned} & \hline 1110 \\ & 1111 \end{aligned}$ | $\begin{aligned} & \hline 0000 \\ & 0000 \end{aligned}$ | $\begin{aligned} & 0011 \\ & 1001 \end{aligned}$ |  |  |
|  |  |  |  |  |


| U | V | X | X-1 |
| :---: | :---: | :---: | :---: |
| 0000 | 0000 | 1100 | 0 |
| 0000 | 0000 | 0110 | 0 |
| 0000 | 0000 | 0011 | 0 |
| 1110 | 0000 | 0011 | 0 |
| 1111 | 0000 | 1001 | 1 |
| $\underline{1111}$ | 1000 | 1100 | 1 |

We have finished four cycles, so the answer is shown, in the last rows of $U$ and $V$ which is: $11111000_{\text {two }}$

Note: By the fourth cycle, the two algorithms have the same values in the Product register.

